



**SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY :: PUTTUR
(AUTONOMOUS)**

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QUESTION BANK (DESCRIPTIVE)

Subject with Code: Computer Organization & Architecture(20CS0504)

Year & Sem : II B.Tech & I-Sem

Course & Branch : B.Tech - CSE, CSIT, CSM, CIC

Regulation : R20

UNIT –I

BASIC STRUCTURE OF COMPUTERS

| | | | | |
|-----------|---|---|-----------|-------|
| 1 | a | Define Computer architecture, organization and list basic functional units in Computer. | [L1][CO1] | [04M] |
| | b | Sketch the basic functional unit of computer and explain each unit in detail. | [L3][CO2] | [08M] |
| 2 | a | Differentiate between I/O unit and memory Unit. | [L4][CO6] | [04M] |
| | b | Describe in detail about the Basic Operational Concepts with neat diagram | [L2][CO1] | [08M] |
| 3 | a | Discuss on basic I/O operations. | [L2][CO1] | [06M] |
| | b | Discuss about Bus structure with neat sketch. | [L2][CO1] | [06M] |
| 4 | a | Illustrate the types of Bus. | [L3][CO1] | [06M] |
| | b | Identify various steps of instruction cycle. | [L3][CO1] | [06M] |
| 5 | a | Demonstrate the Instruction Cycle with neat diagram. | [L2][CO1] | [08M] |
| | b | Differentiate between fetch cycle and execute cycle. | [L4][CO1] | [04M] |
| 6 | a | List out the Computer Instructions and Explain about it. | [L1][CO1] | [06M] |
| | b | Explain in detail about Data Transfer Instructions. | [L2][CO2] | [06M] |
| 7 | | Assess the Data Manipulation Instructions and their types. | [L5][CO1] | [12M] |
| 8 | a | Describe the Arithmetic Instructions with example. | [L2][CO1] | [06M] |
| | b | Illustrate Logical instructions with example. | [L3][CO1] | [06M] |
| 9 | a | Discuss about Program counter and Memory Address register. | [L2][CO3] | [04M] |
| | b | Explain Program Control Instructions. | [L2][CO1] | [08M] |
| 10 | | Illustrate the addressing modes with neat sketch. | [L3][CO3] | [12M] |

UNIT –II**DATA REPRESENTATION & COMPUTER ARITHMETIC**

| | | | | |
|-----------|---|--|-----------|--------------|
| 1 | a | Illustrate the signed number representations | [L3][CO3] | [06M] |
| | b | Explain fixed point representations | [L2][CO3] | [06M] |
| 2 | a | Compare fixed and floating point representations. | [L5][CO1] | [08M] |
| | b | Describe about Character representation. | [L2][CO1] | [04M] |
| 3 | a | Develop a Flowchart for Addition and Subtraction. | [L3][CO3] | [04M] |
| | b | Illustrate the steps for Addition and Subtraction with an example. | [L3][CO3] | [08M] |
| 4 | a | Prepare a flowchart for multiplication of positive numbers. | [L6][CO3] | [04M] |
| | b | Illustrate the steps multiplication algorithm with an example. | [L3][CO3] | [08M] |
| 5 | a | Evaluate $(0010)_2$ with $(0011)_2$ using multiplication algorithm. | [L4][CO3] | [06M] |
| | b | Explain about signed and unsigned numbers representation in binary. | [L2][CO1] | [06M] |
| 6 | | Illustrate the steps in Booth multiplication algorithm and Draw the flowchart with an example. | [L3][CO3] | [12M] |
| 7 | | Invent the steps of Division restoring and draw the flow chart with an example. | [L6][CO3] | [12M] |
| 8 | | Show the step by step signed-operand multiplication process using Booth algorithm When (-9) and (-13) are multiplied. Assume 5-bit registers to hold signed numbers and (-9) to be the multiplicand | [L4][CO3] | [12M] |
| 9 | a | Show the steps of signed operand multiplication with example? | [L2][CO1] | [06M] |
| | b | Write an algorithm for the division of floating point number and illustrate with an example. | [L2][CO3] | [06M] |
| 10 | | Describe the Floating point numbers, its operations and implementation. | [L2][CO1] | [12M] |

UNIT –III**REGISTER TRANSFER & MICRO OPERATIONS AND CPU CONTROL UNIT DESIGN**

| | | | | |
|-----------|---|--|-----------|--------------|
| 1 | a | Define register transfer language? Explain in detail. | [L4][CO3] | [06M] |
| | b | Design the block diagram of the hardware that implements the following register transfer statement P: $R2 \leftarrow R1$. | [L6][CO3] | [06M] |
| 2 | a | Summarize the Register Representations and way it is used. | [L5][CO3] | [06M] |
| | b | Construct a 4-line common bus system with a neat diagram. | [L6][CO3] | [06M] |
| 3 | a | Examine the Bus transfer with neat diagram. | [L3][CO3] | [08M] |
| | b | Draw and explain four bit adder-subtractor circuit. | [L2][CO3] | [04M] |
| 4 | a | Illustrate the three-state bus buffers with neat sketch. | [L3][CO3] | [06M] |
| | b | Discuss about binary increment with neat sketch. | [L4][CO3] | [06M] |
| 5 | | Explain in detail about Arithmetic Micro Operations? | [L3][CO3] | [12M] |
| 6 | | Describe about Logic Micro Operations with neat representation? | [L2][CO3] | [12M] |
| 7 | a | Explain shift micro operations and draw 4 bit combinational circuit shifter. | [L3][CO3] | [08M] |
| | b | Differentiate between Hardwired Control and Micro-programmed control. | [L4][CO6] | [04M] |
| 8 | | What is Hardwired Control? Explain in detail with a neat diagram. | [L4][CO6] | [12M] |
| 9 | a | Describe the Micro Programmed Control with a neat sketch. | [L2][CO6] | [06M] |
| | b | Draw and explain typical hardware control unit. | [L2][CO6] | [06M] |
| 10 | | Survey the Address Sequencing with neat diagram. | [L4][CO4] | [12M] |

UNIT –IV
MEMORY ORGANIZATION

| | | | | |
|-----------|---|---|-----------|--------------|
| 1 | a | Assess the Memory Hierarchy with neat sketch | [L5][CO3] | [08M] |
| | b | Differentiate between RAM & ROM? | [L4][CO2] | [04M] |
| 2 | | What is Main Memory and what are the types in it? Explain in detail. | [L4][CO3] | [12M] |
| 3 | | Categorize the semiconductor RAM in detail. | [L4][CO3] | [12M] |
| 4 | a | Distinguish between SRAM & DRAM? | [L4][CO2] | [04M] |
| | b | Discuss briefly about synchronous DRAMs? | [L2][CO3] | [08M] |
| 5 | a | Classify in detail about ROM. | [L4][CO3] | [04M] |
| | b | Compare the various cache mapping techniques. | [L2][CO4] | [08M] |
| 6 | a | Define Cache Memory? Explain in detail its mapping functions. | [L3][CO4] | [08M] |
| | b | Explain about hit and miss in the memory? | [L2][CO4] | [04M] |
| 7 | a | What is Virtual Memory? Discuss how paging helps in implementing virtual memory. | [L2][CO4] | [08M] |
| | b | What is the need of a page replacement? Discuss the LRU page replacement algorithm with an example. | [L2][CO3] | [04M] |
| 8 | a | Compare various types of Auxiliary memory. | [L2][CO2] | [06M] |
| | b | Define track and sector. Analyze the importance of auxiliary memory? | [L4][CO3] | [06M] |
| 9 | | Describe the use of DMA controllers in a computer system with a neat block diagram. | [L2][CO6] | [12M] |
| 10 | a | Describe in detail about the DMA operations with neat diagram. | [L2][CO6] | [06M] |
| | b | Give detailed notes on DMA transfers with neat sketch. | [L4][CO6] | [06M] |

UNIT –V**PIPELINING & PARALLEL PROCESSORS**

| | | | | |
|-----------|---|---|-----------|-------|
| 1 | | Describe the concept of Pipelining with clear example. | [L2][CO5] | [12M] |
| 2 | a | Explain in detail about basic pipeline processing? | [L2][CO6] | [06M] |
| | b | Sketch the arithmetic pipeline for floating point multiplication? | [L3][CO5] | [06M] |
| 3 | a | Anticipate the conflicts in pipelining and describe about it. | [L6][CO5] | [06M] |
| | b | Illustrate the instruction pipeline with neat timing diagram. | [L3][CO5] | [06M] |
| 4 | a | Construct 4-segment Instruction Pipeline and explain. | [L6][CO5] | [06M] |
| | b | Define the hazards? Explain in detail about instruction hazards? | [L3][CO1] | [06M] |
| 5 | | Categorize and discuss various forms of parallel processing based on Flynn's taxonomy with a neat sketch. | [L4][CO5] | [12M] |
| 6 | a | Visualize the characteristics of Multiprocessor. | [L1][CO5] | [06M] |
| | b | Implement three types multiprocessor system with neat sketch. | [L6][CO5] | [06M] |
| 7 | | Describe the Interconnection Structures in detail. | [L3][CO6] | [12M] |
| 8 | a | Sketch 8×8 omega switching network and explain it. | [L3][CO6] | [06M] |
| | b | Express about crossbar switch with neat sketch? | [L2][CO6] | [06M] |
| 9 | a | What is multistage network? Appraise it with neat sketch. | [L5][CO6] | [06M] |
| | b | Analyze about the hyper cube network with neat sketch? | [L4][CO6] | [06M] |
| 10 | | Illustrate the cache coherency. | [L4][CO6] | [12M] |

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